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Research and Development of Silicon Carbide (SiC) Avalanche Sharpeners for Picosecond Range, High Power Switches

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14. ABSTRACT

This report results from a contract tasking Ioffe Institute as follows: The Grantee will develop, fabricate, test, and characterize 4H-SiC power semiconductor switches operating in picosecond range of switch time. Special 4H-SiC multi-layered junction structures, such as diode structures (p+nn+-type) and triode structures (p+np+- and n+pn+-type) will be fabricated and tested as avalanche sharpeners.

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1. Executive summary

I. A simple analytical model for fast impact ionization front (FIIF) in a reversely biased p^+nn^+ structure is developed. Evaluations of performance of prospective 4H-SiC closing switches based on propagation of such fronts are made. The model allows an estimate of the order of magnitude values of the front velocity and the electron-hole plasma concentration behind the front to the basic material and structural parameters to be made. We show that high avalanche breakdown field and impact ionization rate of wide bandgap 4H-SiC can lead to dramatic improvement of switching characteristics with respect to Si structures currently used in pulse power applications. The concentration of electron- hole plasma generated by the front passage is of the order of 10^{18} cm^{-3} vs. 10^{16} cm^{-3} in Si. The velocity of ionization front in 4H-SiC is estimated to be ~ 10^8 cm/s which is several times higher than in Si.

II. 4H-SiC FIIF-diode design was chosen taking into account the requirements for triggering the FIIF.

III. 1-kV rated 4H-SiC $p^+n_on^+$ diodes were fabricated and tested with respect to the reverse breakdown behavior. Two novel approaches for 4H-SiC epitaxial junction edge termination are proposed. Both methods incorporate high temperature (1700 - 1800°C) boron diffusion from a local implanted source thus compensating n-type dopants at the edge of the diode. Diodes of first type were made with diffusion pn-junctions as floating guard rings (FGRs). Four mesa-type FGRs with a spacing of 1.5 μm were formed using selective reactive ion etching (RIE). Diodes of second type were made using deep RIE to form mesa structures with 10-μm vertical walls. In diodes of both types, very sharp static breakdown was observed at a reverse voltage V_b of 990 - 1060 V. The critical breakdown field is calculated to be 2.7×10^6 V/cm which is very close to the theoretical limit for the parallel plane 4H-SiC p^+n_o junction with n_o-base doped at $(1.9 - 2)\times10^{16}$ cm^{-3}. The leakage current does not exceed 5×10^{-5} A/cm^2 below $0.9\times V_b$. The diodes withstand avalanche current of 1 A/cm^2 that corresponds to the dissipated power of 1 kW/cm^2.

IV. Pulse tests were performed on the diodes fabricated. Input voltage pulses were formed by a special generator based on Si drift step recovery diodes (DSRDs) and Si avalanche sharpeners (SASs). The generator has adjustable pulse amplitude of 3 - 6 kV and pulse rise time of 1 ns and 0.2 ns. All tested 4H-SiC diodes did not stand the tests showing catastrophic failure at specific points within the main junction. Visualization of the diode electroluminescence under reverse and forward bias together with molten KOH etching revealed the presence of threading dislocations and (0001) basal plane dislocations (BPDs). The total density of dislocations is estimated to be $(1 - 3)\times10^4$ cm^{-2}. The space-charge effects were found to restrict the breakdown power density at the dislocation-related microplasmas.

V. Because present-day commercial 4H-SiC wafers and epilayers contain many non-micropipe crystal defects in high densities, multi-amp high voltage avalanche devices like FIIF-diodes seem guaranteed to contain electrical nonuniformities that could potentially impact device operation. But there have been good news. At ICSCRM-2005 conference (September 2005), Cree reported the progress in reducing the density of basal plane defects that cause device failure (see, for example, ***R. Stevenson's report "Cree calls the shots at ICSCRM" published in December's 2005 issue of COMPOUND SEMICONDUCTORS, p. 19***). The proposed techniques convert the majority of BPDs into threading-edge dislocations during the initial stages of epilayer growth, which helps stop BPD dislocations spreading into the epilayers.

2. Introduction

Fast impact ionization front (FIIF) in a semiconductor pn-structure is a peculiar scenario of impact ionization process occuring in a wavelike mode. In Si-based pn-diodes, FIIFs are usually observed when the reverse bias is rapidly increased, above the threshold breakdown voltage, with the voltage ramp of about 1 kV/ns [*I.V. Grekhov, Sol. St. Electr., 32, 923 (1989)*]. The main feature of the FIIF-mode is that very intensive impact ionization produces huge concentration of free carriers in the high-field region. In contrast to conventional breakdown, this concentration exceeds the density of dopants allowing for the electric field to be screened. Due to the screening effect, the high- field region in which intensive ionization occurs moves from cathode to anode as the superfast front. The front velocity is essentially higher than the carrier saturated velocity. The ionization wave produces high-dense electron-hole plasma behind. After the ionization front runs through the base, the diode is switched on and approximately 100-ps rise time voltage pulse is generated in a series load.

The proposed tasks were to fabricate and test FIIF-diodes based on 4H-SiC. SiC belongs to a class of semiconductors commonly known as "wide bandgap". SiC devices should be able to operate at 500°C or higher, a range far beyond Si. The thermal conductivity of SiC exceeds that of copper; thus heat produced by a device is quickly dissipated. The high inertness of SiC to most chemicals implies that SiC devices have the potential to operate in very caustic environments. Of particular importance for design of electronic devices are SiC's high electric field strength and high saturation drift velocity ($2x10^7$ cm/s), thus allowing smaller, more fast devices. Our estimations show that the parameters of FIIF-devices can be substantially improved in case of SiC devices as compared to Si capabilities. We are proposing to use 4H-polytype SiC material in this effort as it is the most readily available electronic SiC material available at this time, with the best-understood properties, and one can obtain substrates plus epitaxial layer(s) of consistently high quality. We expect:

- To increase the speed of switch operation and the specific commutated power. This enhancement in performance is due to a higher 4H-SiC's electric breakdown field. So it is expected for the FIIF to run through the base of 4H-SiC diodes in a shorter time. Besides, several 4H-SiC devices stacked should have lower parasitic inductance as compared to Si based devices.
- To increase the operation frequency repetition. The upper frequency is determined mainly by heating the device because of commutation losses. In particular, some amount of carriers is excited in the base at elevated temperatures thus preventing the formation of over-stressed region. The FIIF-devices formed in 4H-SiC can operate at extremely high temperatures without suffering from intrinsic conduction effects because of the wide energy bandgap. SiC is an excellent thermal conductor. This property enables SiC devices to operate at extremely high power levels and still dissipate the large amounts of excess heat generated.
- To reduce the weight and size of pulse devices. High thermal conductivity allows the devices to be placed very close together, providing high device packing density.
- To achieve the better reliability of the devices due to the unique thermal conductivity and radiation hardness of 4H-SiC.

The following work have been performed in course of the project:

- Performance evaluation of 4H-SiC power switches based on propagation of fast impact ionization fronts (FIIFs)calculations.

- Choice of the diode structure suitable for exitation fast impact ionization fronts.
- Fabrication of the test generator.
- Fabrication of the diodes.
- Electrical characterization at dc.
- Pulse tests.

3. Technical Description of Work Accomplished

- **Performance evaluation of 4H-SiC based power switches based on propagation of fast impact ionization fronts (FIIFs)**

In this Section we start from basic physics of the superfast impact ionization front and use the fundamental dependences of the front velocity and concentration of the generated plasma on the material and structural parameters to estimate the switching characteristics of SiC structures.

Fig. 1 sketches the electric field $E(z,t)$, the electron concentration $n(z,t)$ and the hole concentration $p(z,t)$ in the traveling impact ionization front.

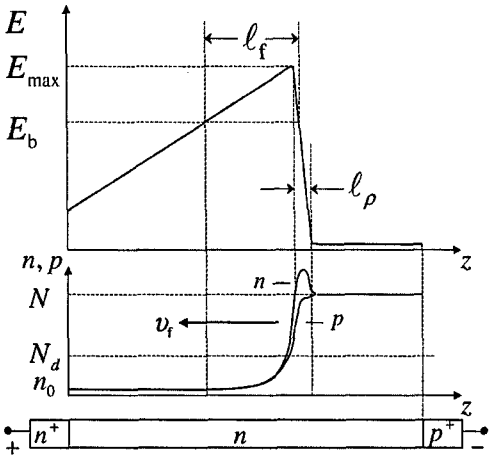

Fig. 1. The electric field $E(z,t)$, the electron concentration $n(z,t)$ and the hole concentration $p(z,t)$ in the traveling impact ionization front.

The n-base of the p^+nn^+-structure is depleted from the major carriers, but there is a small concentration $n_o << N_d$ of non-equilibrium free carriers, where N_d is a doping level in the n-base. To ensure deterministic triggering and propagation of impact ionization front it is required that $n_o > 10^9$ cm^{-3} [***P. Rodin and I. Grekhov, cond-mat/0504638 (submitted to J. Appl. Phys.)***]. The origin of these carriers, often coined as background ionization, will be discussed later. The concentration of electron-hole plasma behind the front, $N >> N_d$, is sufficient to fully screen the electric field. The front passage is a collective process. It is based on avalanche multiplication that increases the concentration of free carriers and Maxwell relaxation that leads to screening of the electric field, whereas drift of individual carriers does not contribute to the expansion of the conducting plasma region. This,

together with the presence of initial carriers in the n-base, makes it possible for the front to travel faster than the saturated drift velocity v_s. The traveling pattern that represents a moving interface between the non-conducting high field region and conducting plasma region is known as a streamer front, or a streamer [***L.B. Loeb, Science, 148, 1417 (1965); E.M. Bazelyan and Yu.P. Raizer, Spark Discharges (CRS, New York, 1998); M.I. D'yakonov and V.Yu. Kachorovskii, Sov. Phys. JETP 67, 1049 (1988); M.I. D'yakonov and V.Yu. Kachorovskii, Sov. Phys. JETP, 68, 1070 (1989); U. Ebert, W. van Saarloos, and C. Caroli, Phys. Rev. Lett., 77, 4178 (1996); Phys. Rev. E, 55, 1530 (1997)***]. An elementary approach to the streamer problem has been originally suggested in Ref. [***M.I. D'yakonov and V.Yu. Kachorovskii, Sov. Phys. JETP 67, 1049 (1988); M.I. D'yakonov and V.Yu. Kachorovskii, Sov. Phys. JETP, 68, 1070 (1989)***] for finger-like streamers in gases and bulk semiconductors and later adapted for planar TRAPATT-like ionization fronts in pn-junctions in Ref. [***A.M. Minarsky and P.B. Rodin, Solid-State Electron. 41, 813 (1997); A.M. Minarsky and P.B. Rodin, Semiconductors, 31, 366 (1997)***].

In 4H-SiC, the impact ionization coefficient for holes is much higher than for electrons. We assume that it is given by a step function:

$$\alpha\ (E) = \alpha_o \Theta(E - E_b) \tag{1}$$

where we take $E_b = 2\times10^6$ V/cm as the effective threshold of impact ionization in 4H-SiC and assume $\alpha_o = 10^5$ cm^{-1} and $\Theta(E)$ is the unit step function. For the electric fields relevant to the impact ionization the carriers drift with saturated velocity $v_s = 2\times10^7$ cm/s. Hence the impact ionization term takes the form $G = \alpha_o v_s n \Theta(E - E_b)$. As it is evident from Fig. 1, the length of this impact ionization region, l_f, where $E > E_b$ is determined by the maximum electric field E_{max} and the slope of the electric field in the depleted region, $dE/dz = qN_d/\varepsilon$

$$l_f \sim \frac{\varepsilon(E_{max} - E_b)}{qN_d} \tag{2}$$

Let us think of the front motion as of discrete two-step process: first the free carrier concentration in the impact ionization region increases uniformly from the initial background concentrations n_o, p_o to the final plasma concentration N, and then the front moves ahead at the distance l_f . In this consideration we neglect the actual spatial profile of electron and holes concentrations in the impact ionization region. The time τ_f it takes for the concentration to increase from n_o to N follows from $N = n_o \exp(\beta\tau_f)$, where $\beta = \alpha_o v_s$ is the ionization frequency. This yields:

$$v_f = \frac{l_f}{\tau_f}, \quad \tau_f = \frac{1}{\alpha_o v_s} \ln\left(\frac{N}{n_o}\right) \tag{3}$$

The concentration N can be determined as follows: we take into account that the planar traveling front carries a sheet charge density $\rho = \varepsilon E_{max}$ which screens the electric field E_{max}. In our two-step model, the front moves ahead at the distance l_f when this space charge ρ has been carried through the impact ionization region:

$$\rho = \int_{o}^{\tau_f} j(t)dt, \quad j(t) = qv_s n_o \exp(\beta t) \tag{4}$$

This yields for the **plasma concentration** N the following formula:

$$N \sim \alpha_o \varepsilon E_{\max} / q \sim \alpha_o \varepsilon E_b / q \tag{5}$$

Hence the order of the magnitude value of the plasma concentration N created by the front passage depends only on the basic material parameters. Combining Eqs. (2) - (5) we obtain the following formula for the **front velocity** v_f:

$$v_f \sim v_s \frac{N}{N_d}\left(\frac{E_{\max}}{E_b} - 1\right)\frac{1}{\ln(N/n_o)} \tag{6}$$

The maximum electric field $E_{\max}$ depends on the specific triggering mechanism and can not be determined by elementary means. $E_{\max}$ enters the model as an external input parameter. In Si and GaAs structures typically $E_{\max} = 1.5E_b$ [***I.V. Grekhov and A.F. Kardo-Susoev, Sov. Tech. Phys. Lett., 5, 395 (1979); Zh.I. Alferov, I.V. Grekhov, V.M. Efanov, A.F. Kardo-Sysoev, V.I. Korol ' kov, and M.N. Stepanova Sov. Tech. Phys. Lett., 13, 454 (1987)***]. Hence

$$E_{\max} - E_b \approx (qN_d / \varepsilon\alpha_o)\ln(N/n_o) \tag{7}$$

Simple expressions obtained connect the material and structural parameters to the the main characteristics of the switching process. The concentration of electron-hole plasma generated by the front passage in 4H-SiC based structure is $N^{SiC} \sim 10^{18}$ cm^{-3} which by 2 orders of magnitude larger than in Si. For the moderate "overstress" $E_{max}/E_b = 1.1$ and $N_d = 10^{15}$ cm^{-3} we find $v_f^{SiC} = 7\times10^7$ cm/s that is several times faster than v_f^{Si}. This front velocity corresponds to the switching time below 10 ps for the n-base width ~ 10 μm. In such regime the actual steepness of the output voltage pulse is determined by the parasitic circuit inductance rather than by switching time of the semiconductor element.

In Si and GaAs structures the front is triggered when the applied reverse bias increases as $V(t) = V_0 + At$, where $V_0 < V_b$ is the initial bias and A is the voltage ramp. It is necessary that $A > 1$ kV/ns. There are two physical reasons why a high voltage ramp is required. First, the avalanche breakdown field E_b should be overcome before a substantial amount of thermal carriers appears in the depleted n-base. This prevents the development of common avalanche breakdown scenario. Second, high voltage rise rate ensures that at the stage of front triggering, when $n,p < N_d$, the edge of impact ionization region where $E > E_b$ moves with velocity v^* that exceeds v_s . Therefore for $v^* > v_s$ all avalanche carriers are trapped in the expanding impact ionization region enabling the formation of the initial nucleous of electron-hole plasma that screens the electric field. For abrupt pn- junctions the condition $v^* > v_f$ is approximately equivalent to $dV/dt > E_b v_s$. This gives the upper bound for the voltage rise rate. For Si it predicts $(dV/dt^{Si})_c > 2$ kV/ns whereas in experiments $(dV/dt)_c > 0.5$ kV/ns. For SiC

we find the **critical voltage ramp** $(dV/dt^{SiC})_c$ to be of about 10 kV/ns. Such high voltage ramps are nowadays routinely achieved by pulse power generators based on Si FIIF-diodes.

- **FIIF-diode design**

I. Three main parameters of 4H-SiC FIIF-diode structure, the dopant density N_d in the base, base thickness and active diode area had to be chosen to satisfy some requirements.

i) *The reverse voltage ramp and triggering pulse amplitude.* The dV/dt value must be ~ 10 kV/ns while pulse amplitude must be several times higher than the threshold breakdown voltage V_b.

ii) *The RC-time of recharging of the diode barrier capacitance, C.* With load resistance R = 50 Ohm, RC value must be lower than the reverse voltage rise time.

iii) *The current density in on-state, j.* For 4H-SiC the j value can be as high as 10^5 A/cm^2 [***N.V. Dyakonova et all, IEEE Trans. on Electr. Dev., 46, 2188 (1999)***].

It is important from practical viewpoint that the critical reverse voltage $(dV/dt)_c$ is not affected by the dopant density in the base. Hence, one can increase the N_d value in order to decrease the critical breakdown voltage V_b. But the higher is the N_d value the higher is the displacement current

$$j_d = qN_d v_s \tag{8}$$

which flows through the diode when the reverse voltage is rised. This current develops a "pedestal" on the output voltage pulse. Besides, the higher the N_d value the higher the pn -junction capacitance C will be:

$$C/S = \left(\frac{q\varepsilon N_d}{2V}\right)^{1/2} \tag{9}$$

Here S is the active diode area, q is the electron charge, ε is the dielectric constant, and V is the reverse voltage. For our experiments, we have chosen $N_d = 2\times10^{16}$ cm^{-3} to block stationary reverse voltages $V < V_b$ = 1 kV. The thickness of Space Charge Region (SCR) at a given voltage V,

$$w = \left(\frac{2\varepsilon V}{qN_d}\right)^{1/2} \tag{10}$$

For triggering voltage V_{tr} = 2 - 3 kV, w is calculated to be 10 - 13 μm. To exclude long-wavelength instability of ionization wave, the base thickness d should be 2 - 3 times higher than w [***A.M. Minarsky and P. Rodin. Sol. St. Electr., 41, 813 (1997)***]. We have chosen d = 20 μm.

With dV/dt = 10 kV/ns and V_{tr} = 2 - 3 kV, the voltage rise time Δt_r must be 150 - 200 ps. For RC < 50 ps, the initial diode capacitance C_o must be < 1 pF. This can be obtained for an initial bias of V_o = 500 V if the diode area S is about 10^{-3} см^2 . In this case the displacement current, $I_d = j_d S$ = 30 A ($j_d = 3\times10^4$ A/cm^2), will develop a pedestal of about 1.5 kV. At the current density in on-state of 10^5 A/cm^2 (100-A total current amplitude) the voltage peak of 5 kV can be generated in 50-Ohm load. So, a 5-kV, 200-ps test generator is needed for FIIF triggering.

II. As is widely known, high voltage junctions under reverse bias exhibit significantly lower breakdown voltages than one-dimensional theory predicts due to effects of field crowding at the junction periphery. Specialized edge termination structures must be used to minimize this effect. Several methods for SiC Schottky barrier and pn junction edge termination have previously been investigated such as field plate extensions [*Q. Wahab, T. Kimoto, A. Ellison, C. Hallin, M. Tuominen, R. Yakimova, A. Henry, J.P. Bergman, E. Janzen. Appl. Phys. Lett., 72, 445 (1998)*], junction termination extensions (JTE) [*D.C. Sheridan, G. Niu, J.N. Merrett, J.D. Cressler, C. Ellis, C.-C. Tin. Solid-State Electronics, 44, 1367, (2000); D.C. Sheridan, G. Niu, J.N. Merrett, J.D. Gressler, J.B. Dufrene, J.B. Casady, I. Sankin. Proc. of the Intern. Symp. on Power Semiconductor Devices and ICs, Osaka, 2001, p. 191*], floating guard rings (GRs) [*I. Sankin, J.B. Dufrene, J.N. Merrett, J.B. Casady. Materials Science Forum, 433-436, 879 (2003); X. Li, K.Tone, L. Hui, P. Alexandrov, L. Fursin, J.H. Zhao. Mater. Sci. Forum, 338-342, 1375 (2000); D. Peters, R. Schorner, K.H. Holzlein, P. Friedrichs. Appl. Phys. Lett., 71, 2996 (1997); K.J. Schoen, J.M. Woodall, J.A. Cooper Jr., M.R. Melloc. IEEE Trans. Electron. Dev. 45, 1595 (1998)*].

Proper edge termination is a problem of vital importance for all avalanche-type semiconductor devices. In order to trigger uniform fast impact ionization front, it is important to achieve quasi one-dimensional breakdown like that in parallel plane junction. An effective method of reduction of the edge electric field in semiconductor structures is to widen the depletion layer under the junction edge by making a positive bevel or incorporating a region with lower dopant density. Specialized edge termination structures must be used. In Si avalanche sharpeners a positive bevel is usually made by mechanical grinding. This technique is hard to apply to SiC diodes because of their small working area not exceeding 0.1 cm^2 . On the other hand, no dry etching technique is developed yet to form mesa-type structures in SiC with preconfigured wall shape (selective reactive ion etching is known to form only vertical mesa walls in SiC).

We propose two novel approaches for SiC junction edge termination which incorporate high temperature (1700 - 1800°C) boron diffusion from a local implanted source thus compensating n-type dopants at the edge of the diode. The n_0 -type base layer is locally compensated at the diode edge that makes the pn-junction "higher-voltage" as compared to the main junction.

The diffusion of implanted boron in 4H-SiC has been studied by secondary ion mass spectrometry by M.K. Linnarson et all [*M.K. Linnarsson, M.S. Janson, A. Shöner, A. Konstantinov, B.G. Svensson, Materials Science Forum, 457-460, 917 (2004)*]. Three kinds of epitaxial layers have been used, highly p-type, highly n-type and low doped n-type. The redistribution of boron was observed to be radically different in the p-type, n-type, and intrinsic samples. The absolute diffusivity in the p- and n-type layers values were found to differ by four orders of magnitude. The diffusion results in a constant boron level throughout the p-type layer (9 μm) while in the n-type layer the boron profile behaves in a complementary error function (erfc) manner. It is expected that the nitrogen donors in the n_0- layer are partly compensated by boron acceptors.

- **Diode fabrication**

A 4H-SiC epitaxial $p^+n_0n^+$ wafer purchased from Cree, Inc. grown on the research grade n-substrate was used to fabricate the diodes. The net donor concentration of 20-μm thick nitrogen (N)-doped n_0-epilayer was (1.9 - 2)×10^{16} cm^{-3} . The Al-acceptor concentration of p^+-layers and the N-donor concentration of n^+-layers were designed to be 10^{19} cm^{-3}.

		Epitaxy Data										
		Layer 1			Layer 2			Layer 3				
Item #	Wafer	Con	Doping	Thick	Con	Doping	Thick	Con	Doping	Thick		
1	CQ0604-02	N	1e+018	1.00	N	1.8e+016	20.00	P	1.33e+019	1.00		
2	CQ0604-06	N	1e+018	1.00	N	1.97e+016	20.00	P	1.25e+019	1.00		
	Minimum:		1e+018	1.00		1.8e+016	20.00		1.25e+019	1.00		
	Average:		1e+018	1.00		1.86e+016	20.00		1.28e+019	1.00		
	Maximum:		1e+018	1.00		1.97e+016	20.00		1.33e+019	1.00		

Table 1. Specification for 4H-SiC $p^+n_on^+$ epi-structures.

In order to make p^+n_o junctions to be "higher-voltage" at the edge than the main junction, boron acceptors were introduced into the peripheral region of the main junction by local diffusion. In our experiments, the boron diffusion source was introduced into the p^+-layer by room temperature ion implantation of 100-keV boron ions at a dose of ranging from 3×10^{14} cm^{-2} to 1×10^{15} cm^{-2} . An aluminum layer of 1-μm thick was served as a mask during boron implantation. The ring windows of 350-μm inner diameter and 50-μm width were opened in the aluminum layer by the photolithography. Subsequent post-implantation thermal anneals have been carried out in Ar atmosphere at 1700 - 1800°C for 20 min. In our case, it is expected that the nitrogen donors in the n_o-layer are partly compensated by boron acceptors.

FGR structures. The conventional floating guard ring (FGR) structure serves to reduce the amount of field crowding at the main junction by spreading the depletion layer past consecutively lower potential floating junctions. A ring becomes biased when the spreading depletion layer punches through to the floating junction. These independent junctions act to increase the depletion layer spreading, thereby reducing the field crowding at the edge of the main junction (Fig. 2).

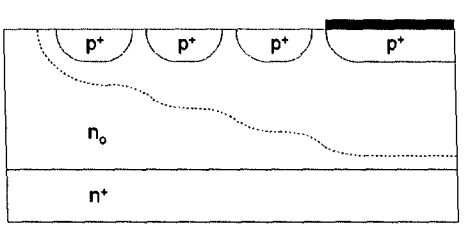

Fig. 2. Schematic diagram of a planar $p^+n_on^+$ diode with multiple floating guard rings.

In SiC based GR structures, the optimum junction-to-ring distance leading to the highest breakdown voltage has to be very narrow compared to the case of a silicon-based structure for the same blocking ability, due to the relatively small thickness of the blocking layer. Indeed for 4H-SiC $p^+n_on^+$ diodes with $N_d = 2\times10^{16}$ cm^{-3} 4 - 20 guard rings (spacing of 2 μm) were tested in Ref. [***I. Sankin, J.B. Dufrene, J.N. Merrett, J.B. Casady, Materials Science Forum, 433-436, 879 (2003)***]. The best diodes demonstrated soft breakdown at 874 V for 4-ring devices and 1100 V for 12-ring devices. The large number of rings may be not an acceptable way for some

fast switch-mode applications because of increased device capacitance. In the case of an avalanche sharpener, the *RC* time should be short enough to provide the necessary ramp of applied reverse voltage. (For 4H-SiC based diodes, the critical voltage ramp is estimated to be 10 kV/ns).

In our case four mesa-type GRs were made from a thin (0.12 μm) Ni layer by lift-off lithography. Individual guard rings were 2 μm wide, the spacing between them being 1.5 μm. Following this, a short surface reactive ion etching was performed to confine the main junction and rings. The backside cathode consists of a thick Ni layer. The resulting FGR structure is shown in Fig. 3.

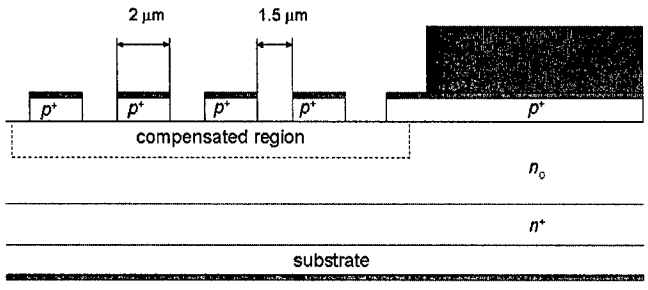

Fig. 3. Schematical cross section of a 4H-SiC FGR-structure fabricated. Dashed line represents a region where nitrogen donors are compensated by boron acceptors.

No intentional surface passivation was performed.

Deep mesa (DM) structures. DM-structures with quasi one-dimensional distribution of the electric field (Fig. 4) were produced by deep RIE of 4H-SiC in SF_6 plasma.

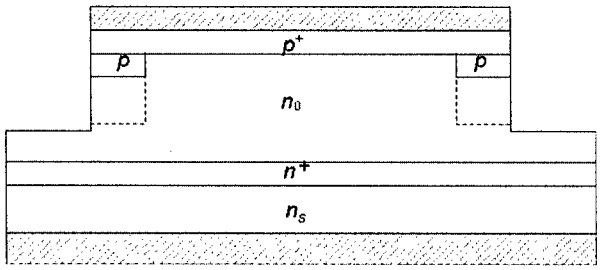

Fig. 4. Schematical cross section of a 4H-SiC DM-structure fabricated. Dashed line represents a region where nitrogen donors are compensated by boron acceptors.

- **Electrical characterization at dc**

Current-voltage measurements were carried out using a probe station and L2-56 curve tracer. The samples were immersed in Perfluoro polyether solution. No special heat-sink cooling was used. Figure 5 show typical

reverse I-V characteristic of 4H-SiC diodes fabricated. Very sharp static breakdown was observed at a reverse voltage of 990 - 1060 V.

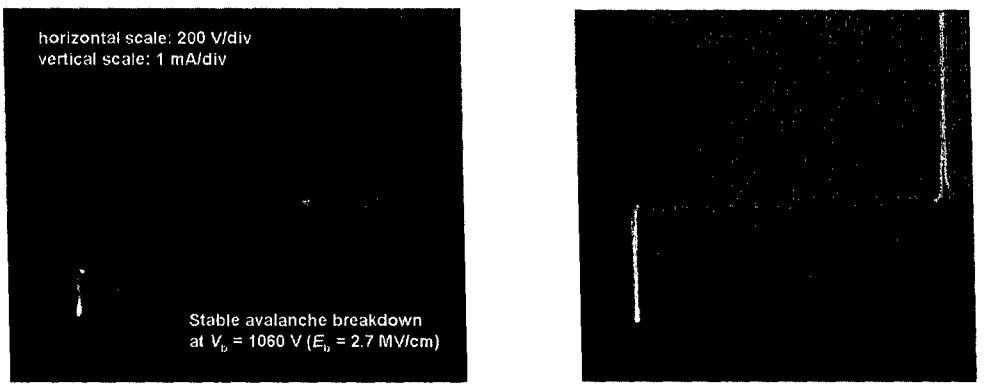

Fig. 5. Current-voltage characteristics of 4H-SiC $p^+n_0n^+$ FGR-(left) and DM-diode (right) showing near ideal low power breakdown behavior. Scales of both oscillograms are same.

The leakage current does not exceed 100 nA (5×10^{-5} A/cm^2) below $0.9\times V_b$ (see Fig. 6). The reverse current starts to increase avalanche-like at about 1060 V then rising with 10 V per decade (note that about 100 V per decade was reported for a conventional guard ring structure; see, for example, [***D.C. Sheridan, G. Niu, J.N. Merrett, J.D. Cressler, C. Ellis, C.C. Tin, Solid-State Electron, 44, 1367 (2000)]***).

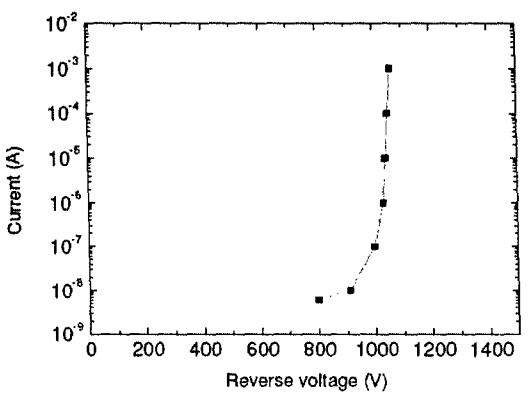

Fig. 6. Reverse current-voltage characteristics of a 4H-SiC $p^+n_0n^+$ FGR-diode.

The stability of the avalanche has been tested in repetitive DC-mode up to 2 mA (1 A/cm^2). The diodes withstand this current without degradation. Note that dissipated power of 1 kW/cm^2 is achieved at 1-A/cm^2 current density. No electroluminescence can be seen at the outer edge of the main junction indicating that the breakdown is located, as expected, in the middle region of the anode.

With the donor density in the n_o-base of (1.9 - 2)×1016 cm^{-3} , the critical value of avalanche breakdown field is calculated from the formula $V_b = \varepsilon E_b^2/2qN$ to be 2.7×10^6 V/cm. In fact, this value is the theoretical limit for the parallel plane 4H-SiC p^+n_o junction with n_o-base doped at (1.9 - 2)×1016 cm^{-3}. Therefore, near ideal breakdown behavior of the diodes is achieved at least for static conditions.

- **Pulse tests**

Pulse tests were performed with the use of an electrical circuit (Fig. 7) build as a 50-Ohm microstrip line.

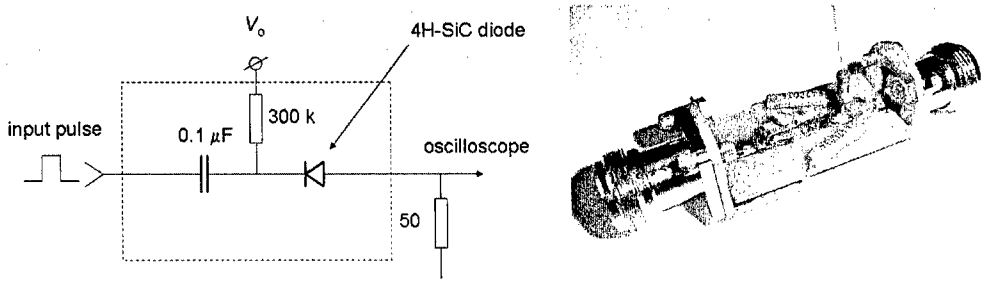

Fig. 7. Electrical circuit used for pulse tests.

Input voltage pulse was formed by test generator. Special test generator based on Si-based DSRD and avalanche sharpeners has been fabricated (Fig. 8).

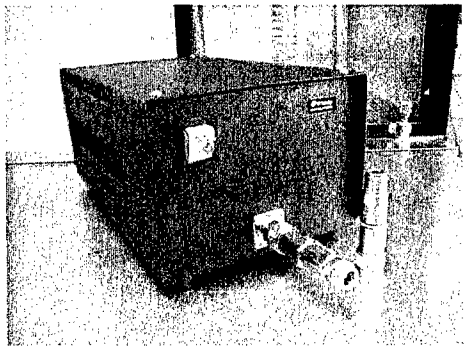

Fig. 8. Photo of the test generator.

The generator has adjustable pulse amplitude of 3 - 6 kV and pulse rise time of about 1 ns and 0.2 ns. The initial reverse dc bias V_o can be applied to the diode through the limiter resistor (300 kOhm). At a voltage V_o = 650 V the initial capacitance of the 4H-SiC diode is about 3 pF providing *RC*-time less than 0.15 ns. The input voltage pulse is applied to the 4H-SiC diode connected in series with 50-Ohm load through the coupling capacitor (0.1 μF). Note that the diodes were stressed by single pulses. The output pulses were recorded by an oscilloscope

(Tektronics TDS 3052B) having 0.7-ns unit-step response. The input pulses with different amplitudes and rise times were applied:

6 kV; 1 ns

6 kV; 0.2 ns

3 kV; 1 ns

3 kV; 0.2 ns.

After each pulse, dc reverse characteristic was checked.

Unfortunately, all tested 4H-SiC diodes did not stand the test showing premature (catastrophic) failure. Figure 9 shows i) input pulses (black curves; these curves were recorded by setting, instead of the 4H-SiC diode, a short-circuiting bridge) and ii) output pulses (color curves). As it can be seen, practically no difference is seen between the input and output pulses for any input pulses (no evidence of breakdown delay was observed in any voltage-time measurements). It proves that each device suffered a substantial sudden increase in current at a reverse voltage slightly above the static breakdown voltage V_b.

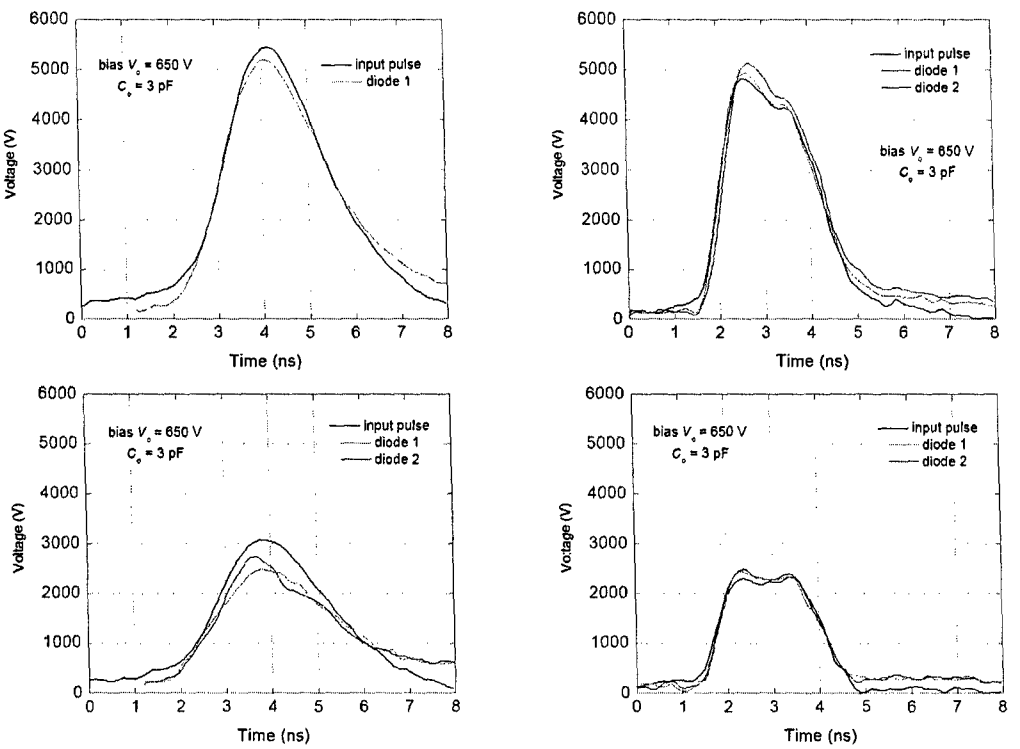

Fig. 9. Typical output pulses illustrating the failure of the diodes.

When the diodes are microscopically observed after pulse test, clear evidence emerges that the junction failure takes place at specific points. The photographs of Fig. 10 shows, for one of the diodes, two highly localized breakdown spots within the bulk junction area.

Note that such local thermal breakdown is developed much faster than the input voltage reaches its maximum amplitude. We believe that the breakdown spots are originated from dislocations of some kind. It is known that space-charge effects restrict the breakdown power density at the dislocation-related microplasmas. Such dislocations can modify the I-V characteristics of diodes, giving rise to higher leakage currents and premature breakdown point-failures.

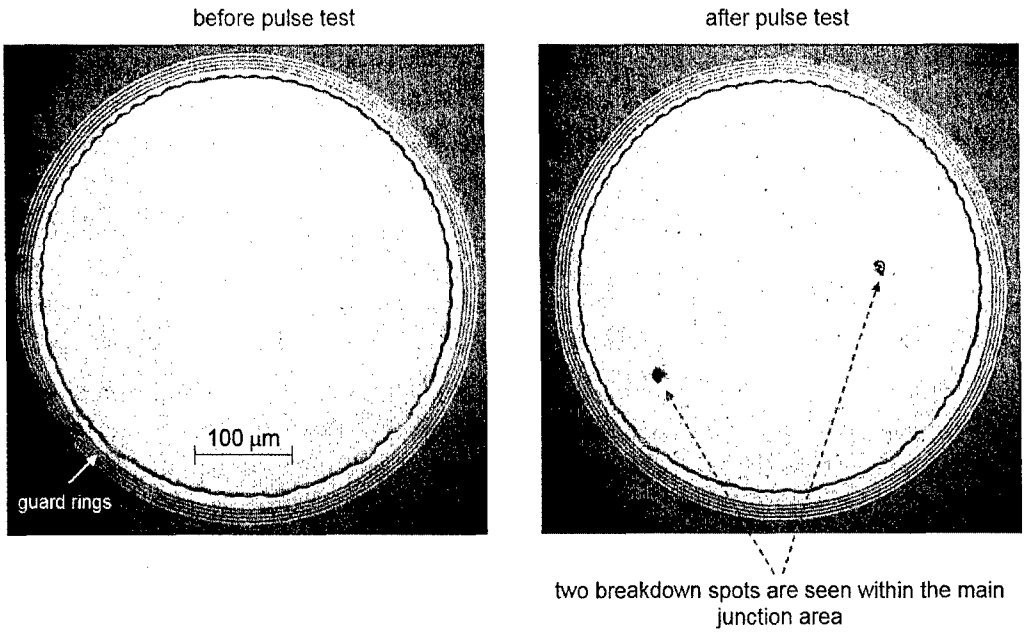

Fig. 10. Plan view of a 4H-SiC FGR-diode showing breakdown spots generated during reverse failure.

Two kinds of defect have been identified in 6H and 4H-SiC, basal plane dislocations (BPD)s, and threading dislocations (TDs) with mostly screw component lying either at a small angle, or parallel, to the c-axis [***S. Ha, W. M. Vetter, M. Dudley, and M. Skowronski, Mater. Sci. Forum, 389–393, 443 (2002); Z. Zhang, Y. Gao, and T. S. Sudarshan, Electrochem. Solid-State Lett. 7, G264 (2004)***]. The BPDs in the SiC epilayer are primarily propagated from the substrate (see Fig. 11).

Usually SiC epilayers are grown on (0001) face substrates with a few degrees off-axis cut. The SiC bulk material contains high-density BPDs, which will intersect the off-cut substrate surface. The typical BPD density in the 8° off-axis (0001) face SiC substrate is ~10^4 cm^{-2} . During conventional epitaxial growth, 70% - 90% of the BPDs in the substrate are converted to become TDs as a result of image force [***J.J. Sumakeris, M. Das, H. McD. Hobgood, S.G. Müller, M.J. Paisley, S. Ha, M. Skowronski, J.W. Palmour, and C.H. Carter, Jr., Mater. Sci. Forum 457–460, 1113 (2004)***]. However, still 10% – 30% of the BPDs in the substrate would propagate into the epilayer, resulting in a BPD density of ~10^3 cm^{-2} in the epilayer. Black points illustrate etch pits formed during the KOH etching (where the BPD intersects the original epilayer surface).

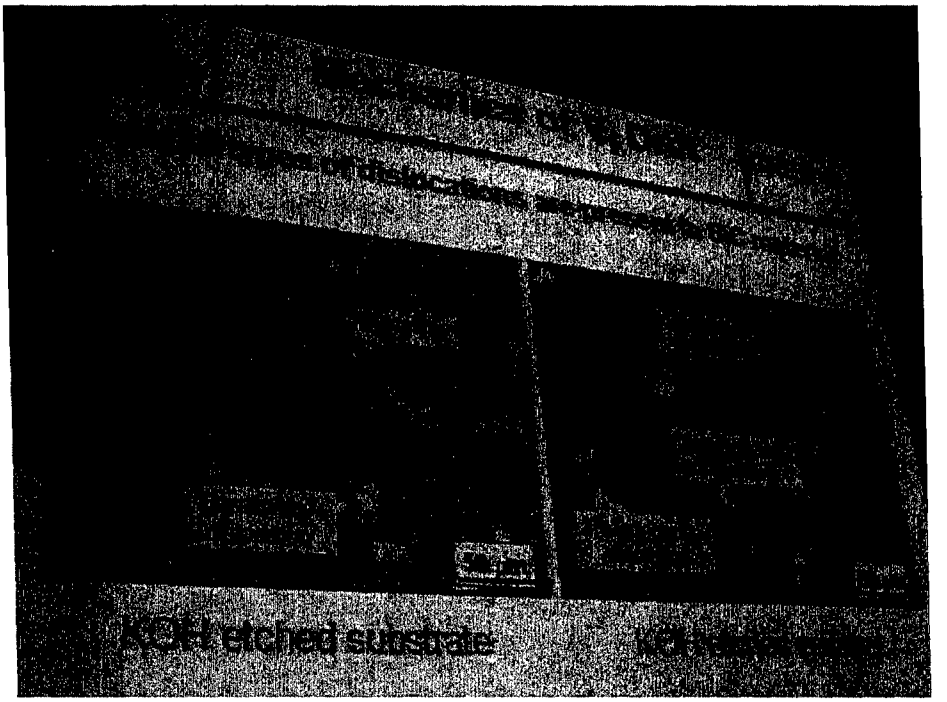

Fig. 11. Micrographs taken of Si-face after KOH etching (presented by Cree at ICSCRM2005, September 2005, Pittsburg PA).

Indeed after molten KOH etching (500°C, 4 min), three kinds of etch pits were observed on the sample surface: large hexagonal, small hexagonal, and shell-like etch pits (Fig. 12), which are identified as TDs and BPDs.

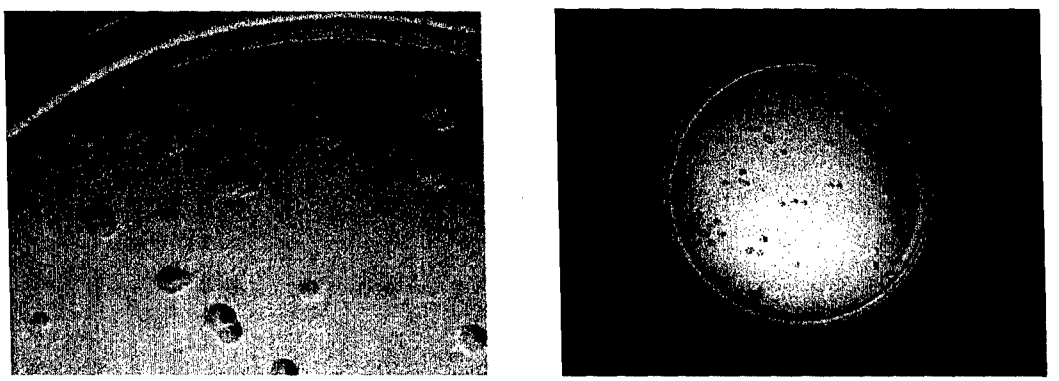

Fig. 12. Etch pits on the surface of a 4H-SiC DM-diode after molten KOH etching (500°C, 4 min).

Besides, the implanted region is clearly seen on the left photo in Fig. 12 as a rough ring. About 50 etch pits can be seen within the 1.3×10^{-3} cm^2 diode area (left photo). This corresponds to the dislocation density of 4×10^4 cm^{-2}. Large hexagonal, small hexagonal, and shell-like etch pits are seen on the right photo which are identified as TDs and BPDs. Dislocations cause an increase in the electric field. As a result, with the reverse bias increasing, the breakdown occurs not across the whole area of the junction but only at at one local point where the field is at its maximum.

In order to prove the dislocation nature of the pulse breakdown, low-energy dc breakdown is optically registered because these defects can be visible as glowing microplasmas. The location of dislocation were recorded by electroluminescence (EL) imaging during the diode operation. Fig. 13 shows EL images under reverse (left) and forward (right) bias (photos were made from the backside through the optically transparent substrate).

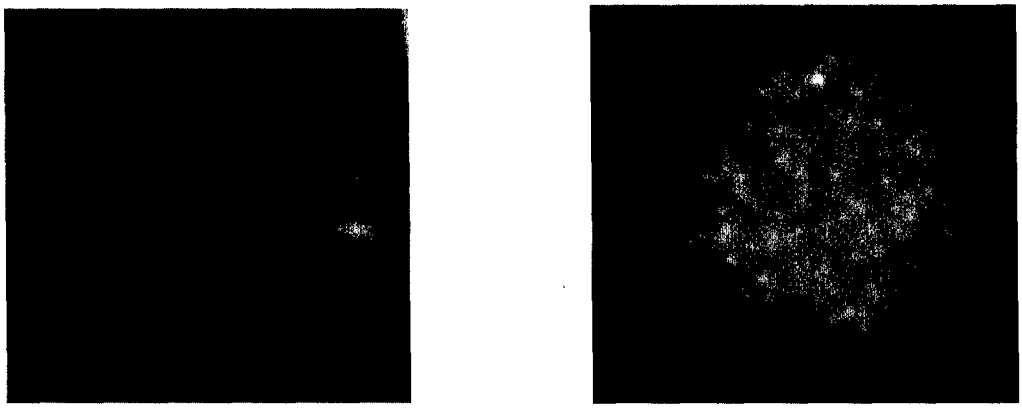

Fig. 13. Visualization of electroluminescence in a 4H-SiC $p^+n_on^+$ DM-diode under reverse (left photo) and forward (right photo) bias.

Under reverse bias, three glowing dislocations are seen while a lot of dislocations can be revealed under forward bias.

4. Conclusions

I. We show theoretically that high avalanche breakdown field and impact ionization rate of the wide bandgap 4H-SiC should lead to dramatic improvement of switching characteristics of 4H-SiC based avalanche sharpeners with respect to Si structures currently used in pulse power applications. The concentration of electron-hole plasma generated by the front passage is of the order of 10^{18} cm^{-3} vs. 10^{16} cm^{-3} in Si. The velocity of ionization front in SiC is ~ 10^8 cm/s that is several times higher as compared to silicon.

II. Two novel approaches for SiC junction edge termination are proposed. One kilovolt-rated 4H-SiC $p^+n_on^+$ diodes are fabricated and tested with respect to the reverse breakdown behavior. Very sharp static breakdown was observed at a reverse voltage of about 1000 V. The critical breakdown field is calculated to be 2.7×10^6 V/cm which is the theoretical limit for the parallel plane 4H-SiC p^+n_o junction with n_o-base doped at 1.9×10^{16} cm^{-3}.

The leakage current does not exceed 5×10^{-5} A/cm^2 below 1000-V reverse voltage. The diodes withstand, without degradation, avalanche current of 1 A/cm^2 that corresponds to the dissipated power of 1 kW/cm^2.

III. Because present-day commercial SiC wafers and epilayers contain many non-micropipe crystal defects like dislocations, multi-amp, high voltage avalanche devices like FIIF-diodes seem guaranteed to contain electrical nonuniformities that impact high power device operation.

5. Future Work Recommended

At ICSCRM-2005 conference Cree launched 4-inch SiC material, demonstrated how to grow high-quality epitaxial layers with reduced density of basal plane dislocations. Cree has made progress in reducing the density of basal plane defects that cause device failure. Two different approaches have been developed to reducing BPD density. In one approach, called LBPD1, potassium hydroxide is used to etch the surface, then a 30 μm-thick epilayer is grown and the substrate is polished, to achieve BPD densities below 10 cm^{-2}. Alternative LBPD2 process produces BPD densities of typically 20 cm^{-2} by hexagonal lithographic patterning of the substrate before growth. Both techniques convert the majority of BPDs into threading-edge dislocations during the initial stages of epilayer growth, which helps stop BPD dislocations spreading into the epilayers.

It is recommended that the work on 4H-SiC based avalanche sharpeners continue when epitaxial material with the density of dislocations not higher than 100 cm^{-2} is readily available.

6. Papers and presentations

1. Pavel Rodin, Pavel Ivanov and Igor Grekhov. "Performance evaluation of picosecond high voltage power switches based on propagation of superfast impact ionization fronts in SiC structures". The manuscript has been accepted for publication in the Journal of Applied Physics, assigned the nine-character AIP ID number 008602JAP, and forwarded to AIP, tentatively scheduled for publication in the January 15, 2006 issue.
2. P.A. Ivanov, I.V. Grekhov, N.D. Il'inskaya, and T.P. Samsonova. "Ideal" Static Breakdown in High-Voltage (1 kV) 4H-SiC Junction Diodes with Guard Ring Termination". Semiconductors, Vol. 39, No. 12, 2005, pp. 1426–1428. Translated from Fizika i Tekhnika Poluprovodnikov, Vol. 39, No. 12, 2005, pp. 1475–1477.
3. P.B. Rodin, P.A. Ivanov, I.V. Grekhov. "Performance evaluation of 4H-SiC power switches based on propagation of fast impact ionization fronts". To be presented at AMEREM, July 2006, Albuquerque NM.
4. I.V. Grekhov, P.A. Ivanov, P.B. Rodin, T.P. Samsonova. "Reverse breakdown tests of 1-kV 4H-SiC $p^+n_0n^+$-diodes made from commercial epitaxial material". To be presented at AMEREM, July 2006, Albuquerque NM.